

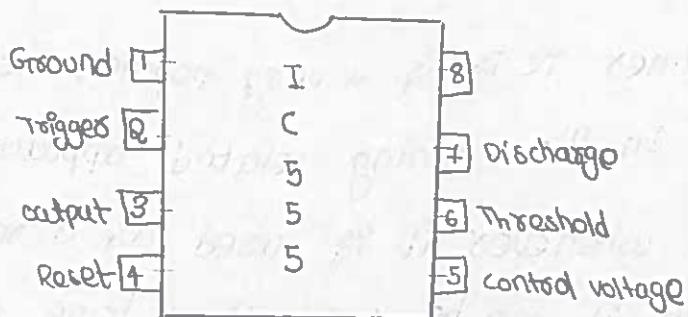
## Timers and phase locked loops

## IC 555 Timer :-

- \* This 555 timer IC is a very popular IC and it is very useful in the timing related applications.
- \* For example whenever it is used as a relaxation oscillator, then it can be used as a tone and alarm generator.
- \* And it can be used for the frequency division or for generating the timing delays.
- \* This is available in so many packages.
- \* The 555 timer is a highly stable device for generating accurate time delay or oscillators.
- \* "Signetics Corporation" first introduced this device as the SE 555 / NE 555 and it is available in two package styles.
- \* Package styles
  - 8 pin circular style
  - 8 pin min DIP (SO) or 14 pin DIP.
- \* The 556 timer contains two 555 timers and it is a 14 pin DIP.
- \* A single 555 timer can provide timedelay ranging from picoseconds to hours, whereas a counter timer can have maximum timing range of delay.
- \* The 555 timer can be used with supply voltage in the range of +5V to +18V can drive up to 200mA.
- \* Because of this wide range of supply voltage, the 555 timer is easy to use in various applications.

- \* The various applications like oscillators, pulse generator, Ramp and square wave generator, Mono-shot multivibro etc., burglar alarm, traffic light control & voltage monitor etc.

→ Pin diagram of IC timer.



Pin 4 :- Ground

- \* All the voltages are measured w.r.t to this terminal.

Pin 3 :- output

- \* The complementary signal output ( $\bar{Q}$ ) of the flip flop goes to pin 3 which is the output.
- \* The load can be connected in two ways.
- \* One is in between pin 3 & GND and other is in between Pin 3 & Pin 8.

Pin 2 :- Trigger

- \* The IC 555 timer uses two comparators C-L & C-Q.
- \* The voltage divided consists of three equal resistances.

Pin 4 :- Reset

- \* This is an input to the timing device.
- \* Pin 4 provides on/off feature to the IC 555.
- \* This pin 4 will overrides all other functions within the timer when it is momentarily grounded.

## Pin 5 :- Control Voltage Input

- \* In most of the applications, external control voltage  $V_{CP}$  is not used.
- \* This pin connected to -ve terminal of C-1. Due to the voltage dividers ckt, the -ve terminal of C-1 holds the voltage at  $\frac{2}{3}V_{CC}$ .
- \* Due to this, the variable input pulse width output is possible. This is called pulse width modulation which is possible due to Pin 5.

## Pin 6 :- Threshold

- \* This is non-inverting  $V_{CP}$  terminal at C-1 the external voltage is applied to this pin 6.
- \* If threshold  $> \frac{2}{3}V_{CC}$ , C-1 o/p high, F/F set & Q-High, Pin 3 Q-Low.
- \* If threshold  $< \frac{2}{3}V_{CC}$ , C-1 o/p is low, F/F reset & Q-Low, Pin 3 Q-High.

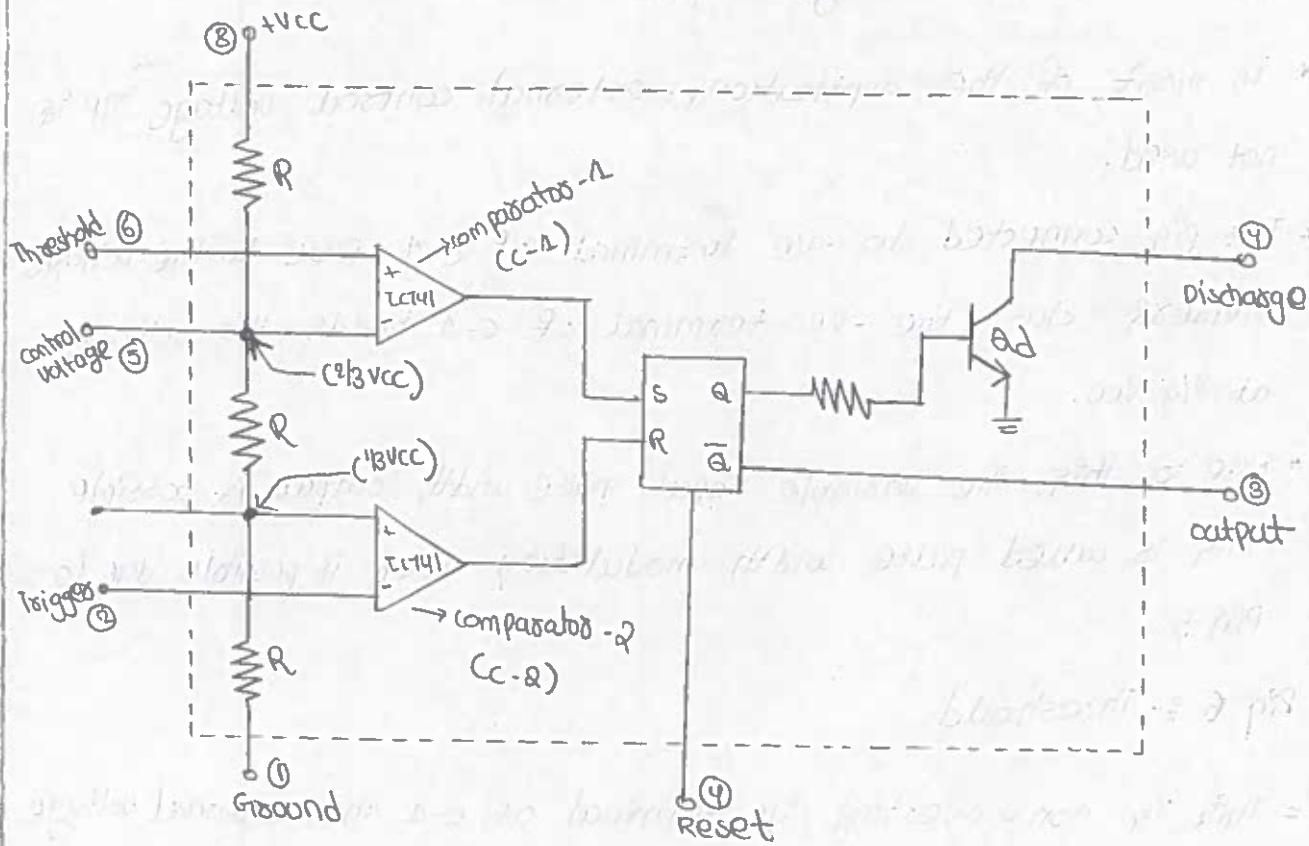
## Pin 7 :- Discharge

- \* This pin is connected at collector of the discharge triac.
- \* When the o/p pin is high, Q is low, due to this triac is off. Now it act as an a.c to the external capacitor C to be connected across it.
- \* When the output pin is low, Q is high, due to this triac is on and it act as s.c, shorting the external capacitor C to be connected across it.

## Pin 8 :- Supply +V<sub>CC</sub>

- \* IC 555 timer can work with any supply voltage b/w 4.5V and 16V.

→ Block diagram of IC555 timer :-



### Features of 555 Timer :-

- i] The 555 is a monolithic timer device which can be used to produce accurate and highly stable time delays or oscillators. It can produce time delays ranging from the few micro seconds to several hours.
- ii] It has two basic operating modes:
  - \* Monostable
  - \* Astable
- iii] It is available in three packages
  - \* 8 pin metal can / circular
  - \* 8 pin mini DIP or 14 pin output
- iv] The NE555 can operate with a supply voltage in the range of 4.5V to 18V and is capable of sourcing and sinking 100mA currents.
- v] It has a very high temperature stability, as it is designed to operate in the temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .
- vi] Its output compatible with TTL, CMOS and op-amp circuits.

# Monostable Multivibrator using IC555 :-

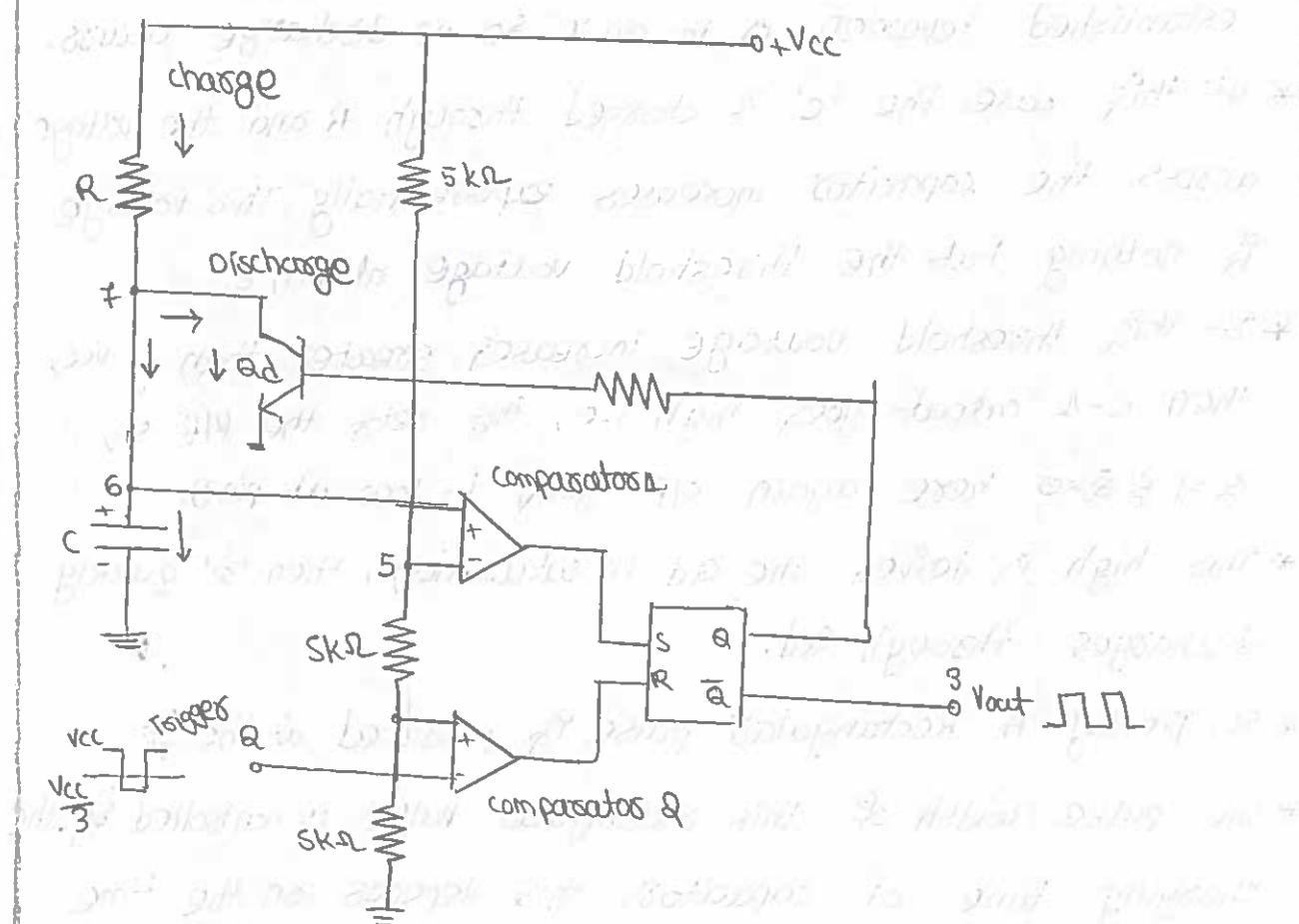


Fig:- Monostable operation of IC555.

The IC555 timer can be operated as a monostable multivibrator by connecting an external R & C.

- \* This ckt has only one stable state
- \* When triggered it produces a pulse at the o/p & return back to its to stable state.

Operation :-

- \* The SR flip-flop is initially set. i.e.,  $Q=1$  then o/p is  $\bar{Q}$  so, the  $\bar{Q}=0$  i.e., o/p is low
- \* Due to  $Q=1$ , the Qd is ON and the external capacitor 'C' discharging to the ground.
- \* When a trigger  $V_{TP} > \frac{1}{3} V_{CC}$  is applied, it triggers  $V_{TP} > \frac{1}{3} V_{CC}$  the o/p of Qd is '0' only. In this case also o/p is not changed at pin 3, it maintains at low only.
- \* When the trigger becomes less than  $\frac{1}{3} V_{CC}$  then the o/p Qd is '1' and QF is having  $Q=0$ ,  $\bar{Q}=1$ . now the o/p at pin 3 is high.

- \*  $RQ_2, Q=0$  then  $Q_d$  is in OFF state, then no connection is established between  $Q$  to pin 4 so no discharge occurs.
- \* At this case the 'c' is charged through R and the voltage across the capacitor increases exponentially. This voltage is nothing but the threshold voltage at pin 6.
- \* If this threshold voltage increases greater than  $\frac{2}{3} V_{cc}$ , then C-I output goes high i.e., this sets the flip-flop so,  $Q=1$  &  $\bar{Q}=0$  here again o/p goes to low at pin 3.
- \* This high  $Q$  drives the  $Q_d$  in saturation, then 'o' quickly discharges through  $Q_d$ .
- \* So, finally a rectangular pulse is produced at the o/p.
- \* The pulse width of this rectangular pulse is controlled by the charging time of capacitor, this depends on the time constant  $RC$ . This  $RC$  controls the pulse width of the o/p signal.

Derivation of pulse width :-

The voltage across capacitor increases exponentially and given by

$$V_C = V(1 - e^{-t/RC}) \quad \text{--- (1)}$$

according to virtual ground concept

$$V_C = \frac{2}{3} V_{cc} \text{ and from the ckt } V = V_{cc}$$

sub  $V_0$  &  $V$  in eqn (1)

$$\frac{2}{3} V_{cc} = V_{cc}(1 - e^{-t/RC})$$

$$\frac{2}{3} = 1 - e^{-t/RC}$$

$$e^{-t/RC} = +\frac{1}{3}$$

$$-t/RC = -1.0986$$

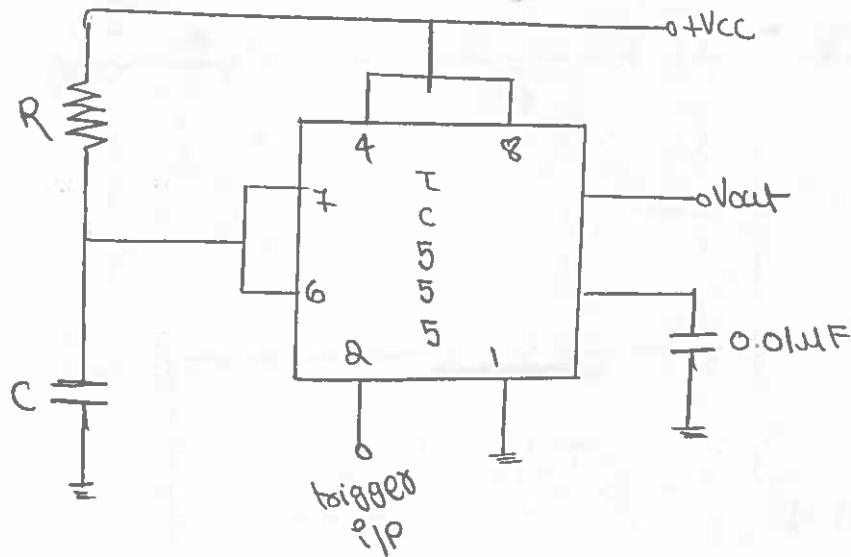
$$t = 1.0986 RC$$

$$t \approx 1.1 RC$$

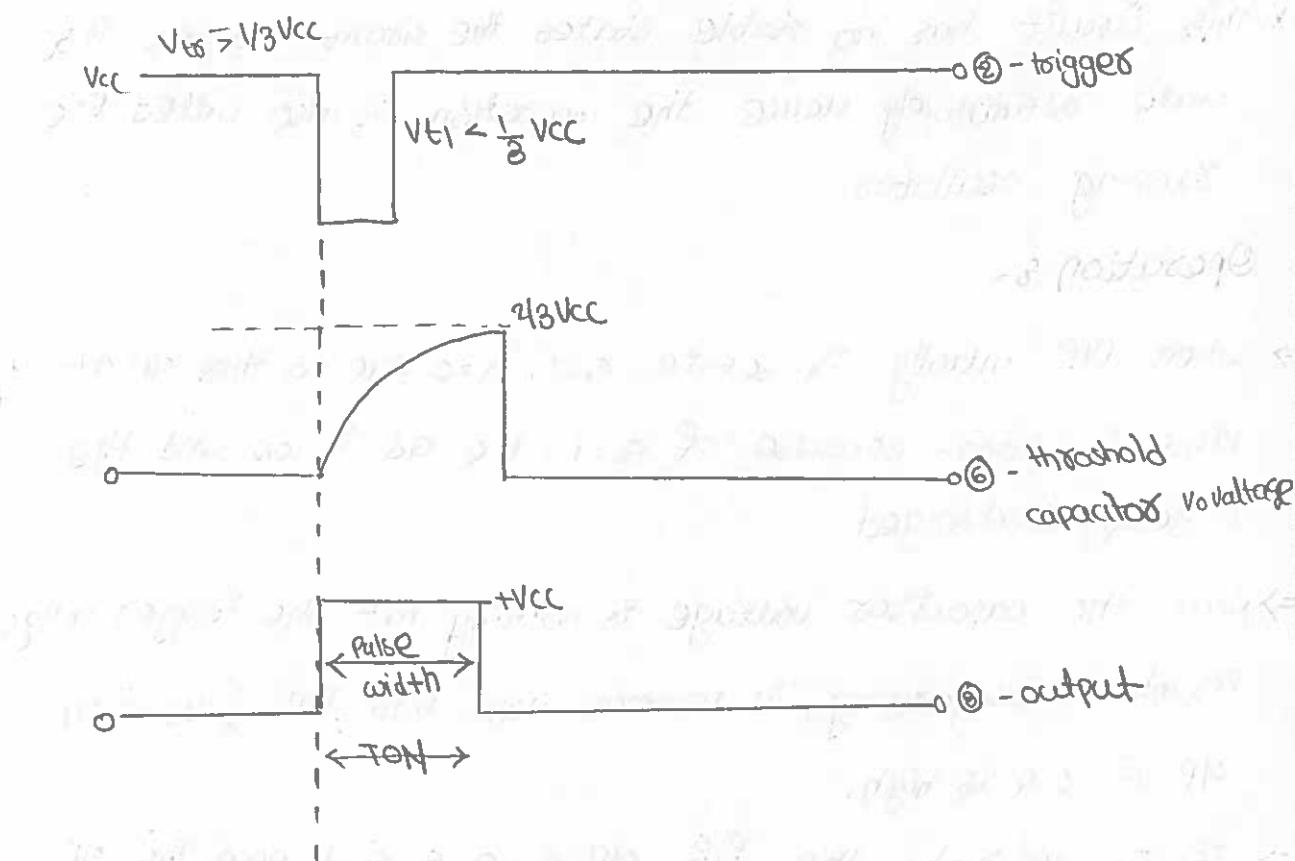
\* So, we can say that voltage across capacitor will reach  $\frac{2}{3} V_{cc}$  in approximately 1.1 times time constant.

$$t \approx 1.1 RC$$

# Schematic Diagram of Nonstable Multivibrator using IC555



- \* The schematic diagram of the IC555 is shown here, which does not include comparators, E/F etc.
- \* It only shows the external components to be connected to the 8 pins of IC555.
- \* Here, the external components are R & C.
- \* To avoid accidental reset, Pin 4 is connected to Pin 8, which is connected to +Vcc.
- \* To achieve the noise filtering of control voltage, the Pin 5 is grounded through a small capacitor of 0.01μF.



# Astable Multivibrator Using IC 555 :-

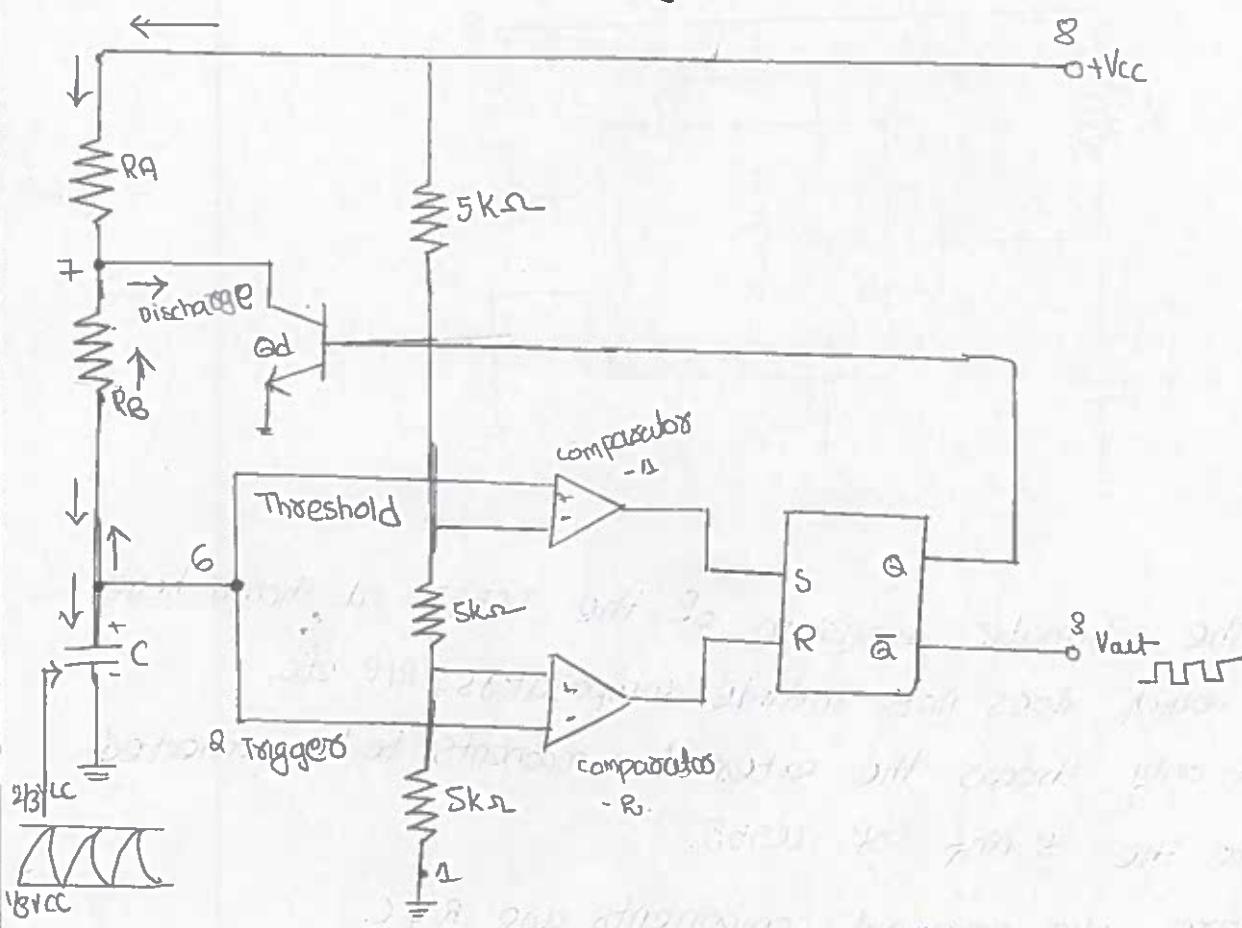


Fig :- Astable Multivibrator.

- \* In this circuit the threshold input & trigger input are connected with each other.
- \* Two external resistors  $R_A$ ,  $R_B$  &  $C$  are used in this circuit.
- \* This circuit has no stable states the circuit changes it's state alternately. Hence the operation is also called free running oscillator.

## Operation :-

- ⇒ When first initially  $Q_1$  is set i.e.,  $Q=1$ ,  $\bar{Q}=0$  due to this o/p at pin 3 is low. Because of  $Q=1$ , the ad is on and the C gets discharged.
- ⇒ Now, the capacitor voltage is nothing but the trigger voltage so, while discharging, it becomes less than the  $\frac{1}{3}V_{CC}$  then o/p of  $C-2$  is high.
- ⇒ If  $C-2$  o/p high, the first o/p  $Q=0$  &  $\bar{Q}=1$ , now the o/p at pin 3 is high.

- ⇒ Because of  $Q=0$ , the QD is off and the capacitor charges through the resistance  $R_A, R_B$ , &  $V_{CC}$ .
- ⇒ Here, the total charging path total resistance is  $(R_A + R_B)$  and the charging time constant is  $(R_A + R_B)C$ .
- ⇒ Now the capacitor voltage is also threshold voltage. If C is charged the threshold voltage is also increases and than the  $\frac{1}{3}V_{CC}$ . At this time the output of C-L is high and the output of flip-flop  $Q=1 \neq \bar{Q}=0$ , i.e., the output at pin 3 is low.
- ⇒ When voltage across C is discharged then trigger O/P is also decreased & the output of C-L is high. Due to this flip-flop output  $Q=0 \neq \bar{Q}=1$ , i.e., the output of pin 3 is high.
- ⇒ Thus, when the output is high, capacitor is charged and when the O/P at pin 3 is low than capacitor is discharged.
- ⇒ The capacitor charges exponentially & O/P of the astable multivibrator is a rectangular waves.
- ⇒ The charging time of the capacitor is given

$$T_C = \text{charging time} = 0.693(R_A + R_B)C$$

- ⇒ While the discharging time is given by

$$T_D = \text{discharging time} = 0.693 R_B C$$

- ⇒ Hence, Positive time for one cycle is

$$T = T_C + T_D$$

$$= 0.693(R_A + R_B)C + 0.693 \cdot R_B \cdot C$$

$$= 0.693(R_A + 2R_B)C$$

$$\text{while } \omega = \frac{1}{T} = \frac{1}{0.693(R_A + 2R_B)C}$$

$$\% \text{ Duty cycle} = \frac{\omega}{T} \times 100$$

$$= \frac{0.693(R_A + R_B)C}{0.693(R_A + 2R_B)C} \times 100$$

$$\% D = \frac{RA + RB}{RA + 2RB}$$

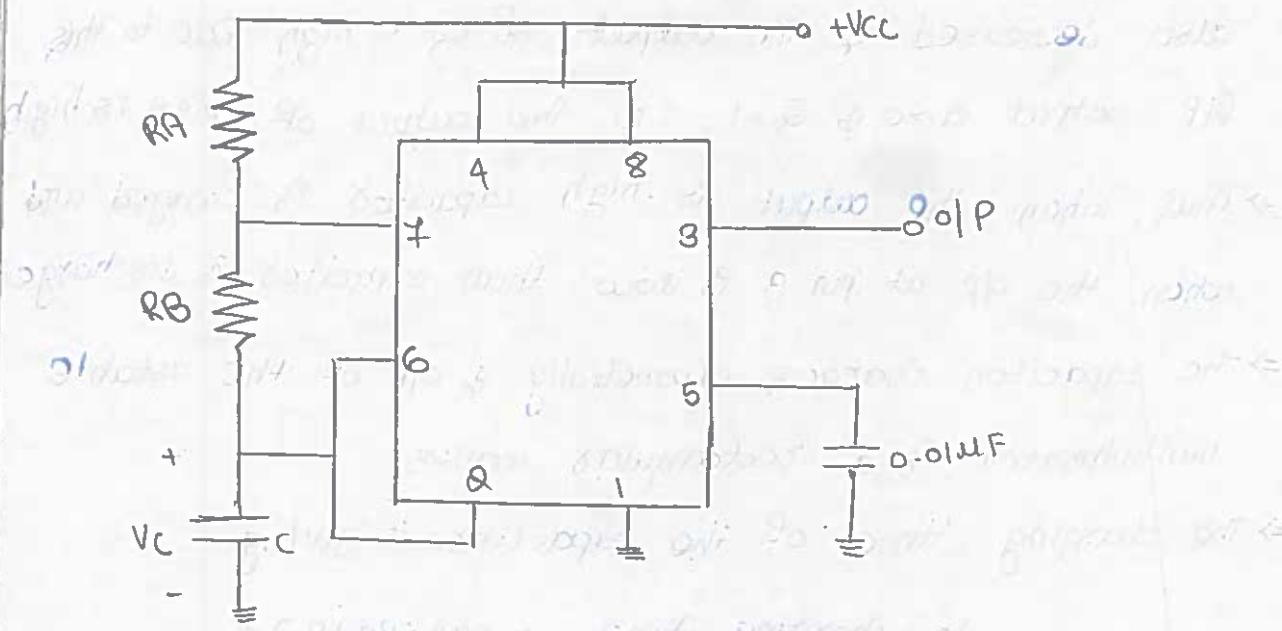
⇒ while the frequency of oscillations is given by

$$f = \frac{1}{T} = \frac{1}{0.693(RA + 2RB)C}$$

$$f = \frac{1.44}{(RA + RB)C}$$

⇒ If  $R_A$  is much smaller than  $R_B$ , then duty cycle approach goes to 50% & output waveform approaches to square wave.

Schematic diagram for IC555 as Astable Multivibrator :-



⇒ It shows only the external components  $R_A$ ,  $R_B$  &  $C$ .

⇒ The pin 4 is tied to pin 8 & pin 5 is grounded through a small capacitor.

⇒ The important application of Astable multivibrator is voltage controlled oscillators (VCO).

⇒ Here, the pin 2 & pin 6 also well connected.

Derivation of duty cycle :-

⇒ Generally the charging time constant is greater than the discharging time constant. Hence at the output waveform is not symmetric.

→ the high output remains for longer period than low output. The ratio of high output period and low output period is given by mathematical parameter called duty cycle.

It is defined as the ratio of ON time i.e., high output to the total time of one cycle.

$$\text{duty cycle } (D) = \frac{w}{T}$$

where  $w$  = time for  $V_{out}$  is high

$$= T_{ON}$$

$$T = \text{Time of one cycle}$$

$$\% D = \frac{w}{T} \times 100 \%$$

one cycle = +ve half + -ve half.

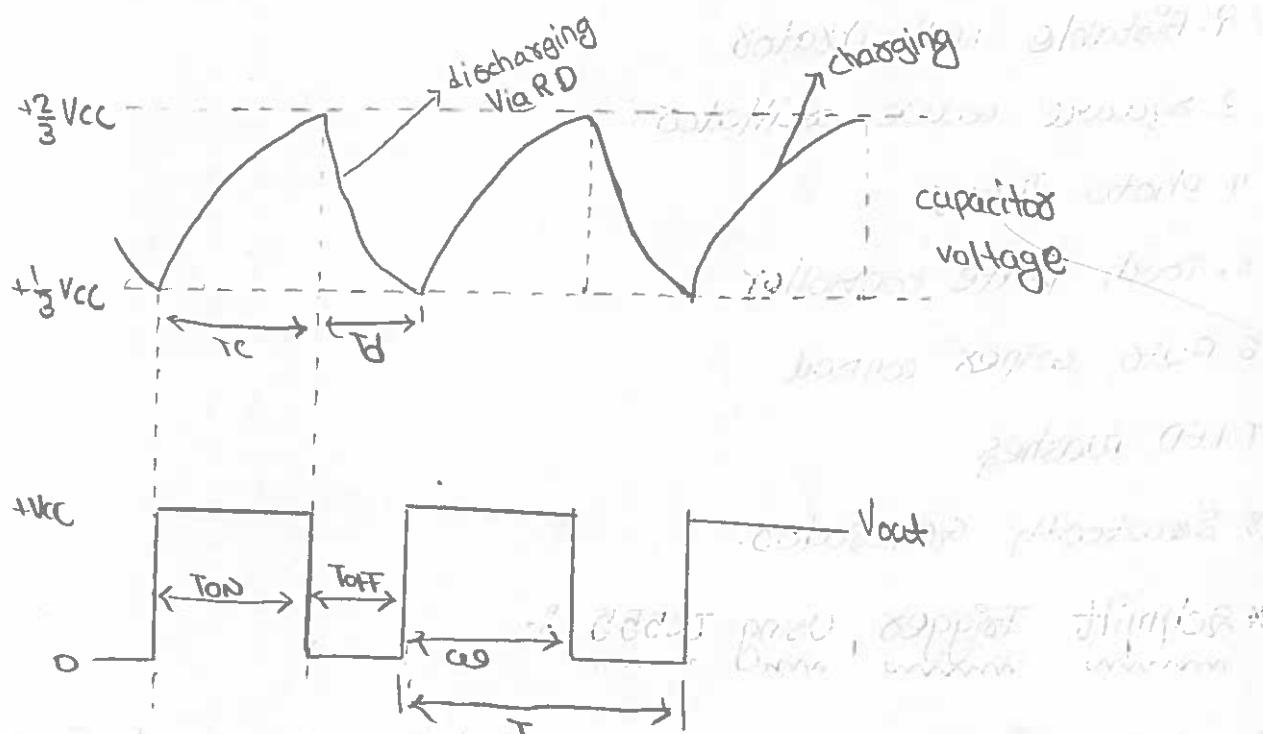


Fig :- waveforms of Astable operators.

## Applications :-

### 1. Applications of Monostable Multivibrator

- Frequency divider
- Pulse width Modulation
- Wave RAMP Generators
- Missing Pulse detector
- Pulse position Modulation (PPM).

### 2. Applications of Astable Multivibrator

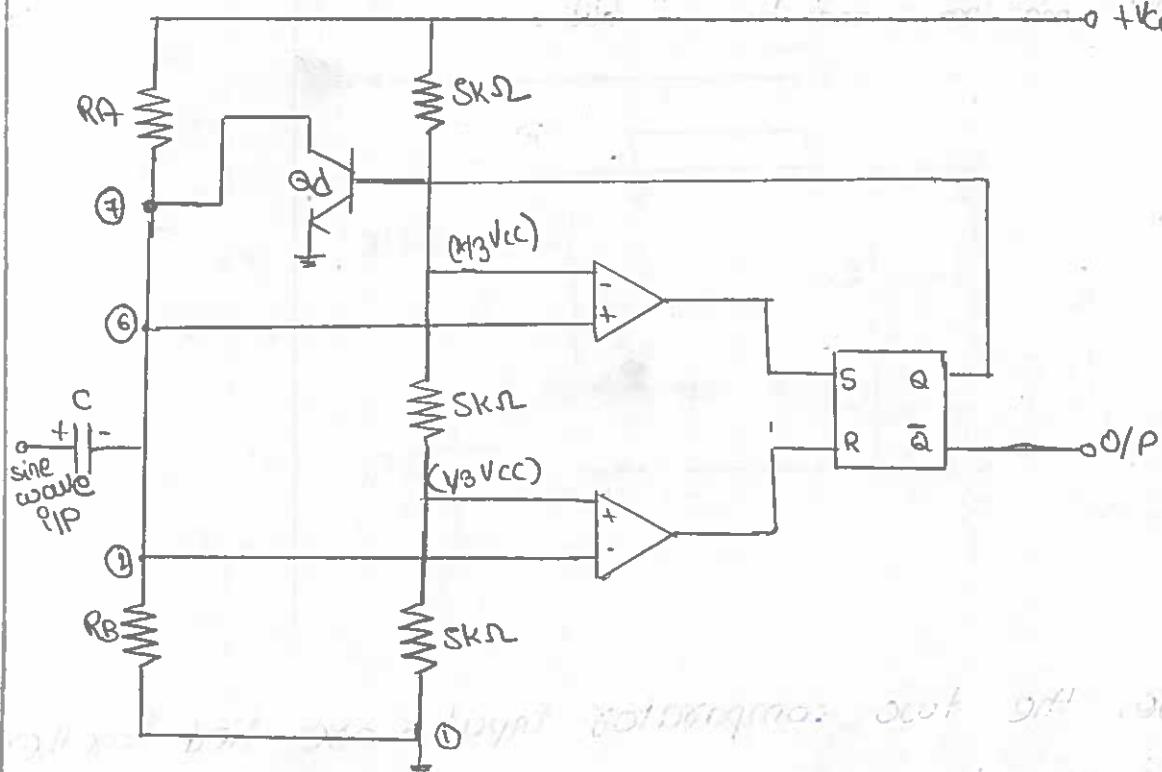
- Square wave Generator
- Voltage controlled oscillator
- FSK generator

### Applications of IC 555 :-

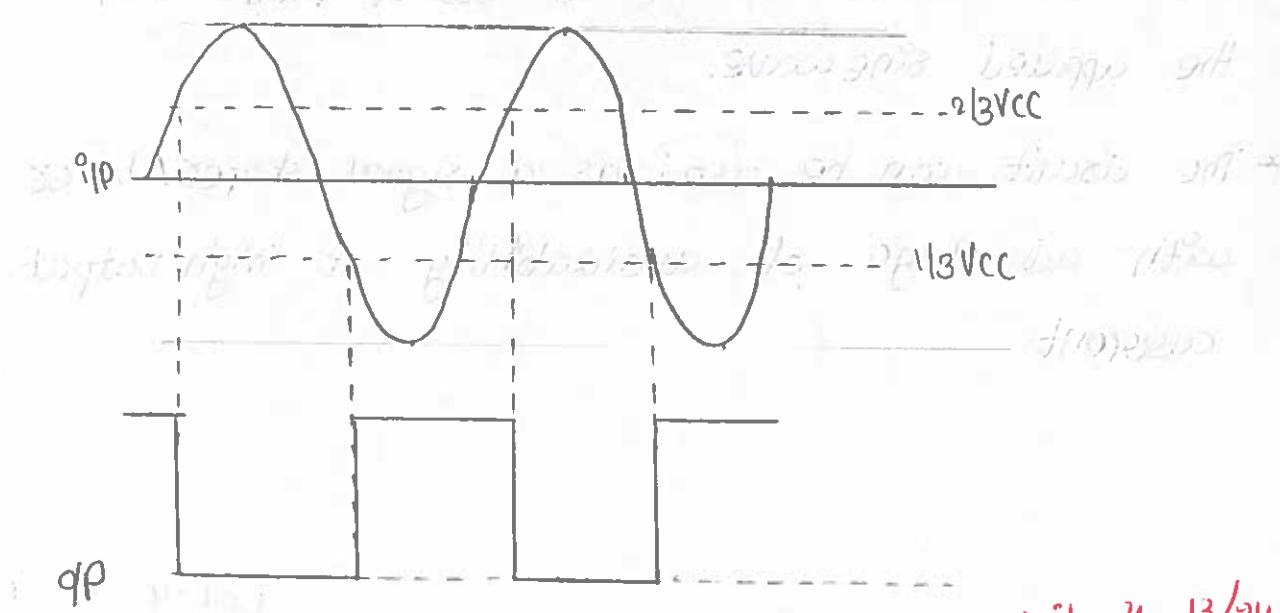
1. Schmitt Trigger
2. Bistable Multivibrator
3. Square wave oscillator
4. Photo Timer
5. Touch plate controller
6. Auto wipers control
7. LED flashes
8. Sawtooth generators.

### \* Schmitt Trigger Using IC 555 :-

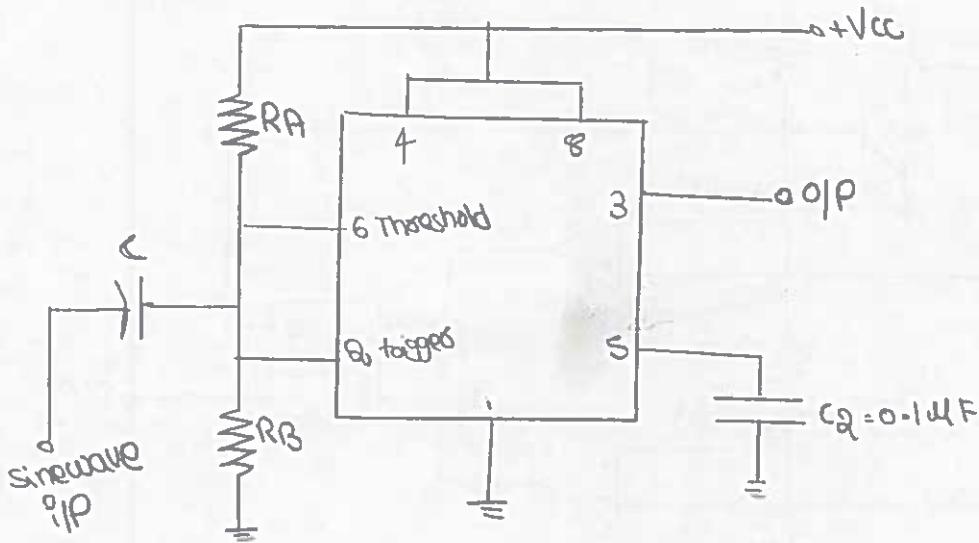
- ⇒ Initially set the pin output at '0'. i.e.,  $Q=0$  and  $\bar{Q}=1$ .  
Now, the output at pin 3 is high.
- ⇒ Due to  $Q=0$  the Qd is in OFF i.e., it is the capacitor is charged with a sine wave.
- ⇒ We know that input for a schmitt trigger is a sine wave.



- If we keep an increasing positive charge at the 'c' the voltage at positive terminal of  $C_1$  is increased due to this positive input  $> \frac{2}{3} V_{CC}$  then output of  $C-1$  is '1'.
- ⇒ Similarly positive voltage at negative terminal of  $C_2$  is also increased due to this negative input  $> \frac{1}{3} V_{CC}$ , now positive output of  $C-2$  is '0'.
- Now, this output is also given to the flip-flop as  $S=1$  &  $R=0$  due to this  $\bar{Q}=0$  &  $Q=1$  i.e., the output at pin 3 is low.
- The output is high when the input reaches to  $\frac{2}{3} V_{CC}$  and output is low when the capacitor decreases upto  $\frac{1}{3} V_{CC}$ .



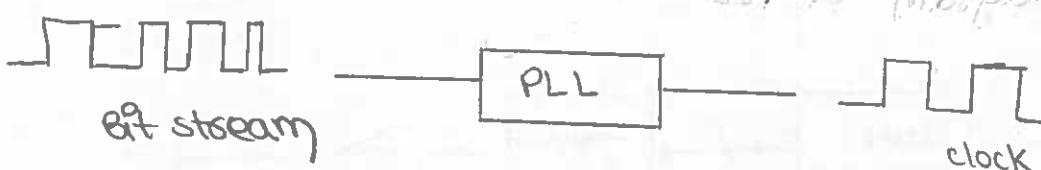
# IC555 as a Schmitt Trigger



- \* Here, the two comparator inputs are tied together and biased at  $\frac{1}{3} V_{CC}$  through a voltage divider  $R_A$  &  $R_B$ .
- \* Since, the threshold comparator will trip at  $\frac{2}{3} V_{CC}$  and the trigger comparator will trip at  $\frac{1}{3} V_{CC}$ , this bias is provided by the  $R_A$  &  $R_B$  is centered within comparators trip limits.
- \* A sine wave input at sufficient amplitude to exceed the reference levels because the internal flip flop to be set and reset.
- \* In this way, it creates a square wave at the output.
- \* So long as  $R_A$  is equal to  $R_B$ , the 555 will automatically biased correctly for almost any supply voltage.
- \* The output waveform is  $180^\circ$  out of phase with the applied sine wave.
- \* The circuit can be used as a signal shaper / buffer with advantage of availability of high output current.

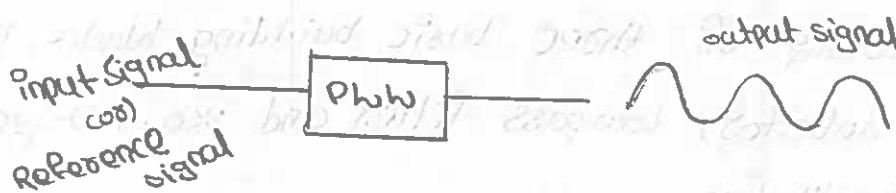
## Phase lock loop :-

- ⇒ The PLL are widely used in many applications are electronics.
- ⇒ In communication, they are used in the synchronization and demodulation circuit for example the FM demodulation and in the FSK, they are commonly used.
- ⇒ In communication system for the jitter & the noise reduction the PLL commonly used.



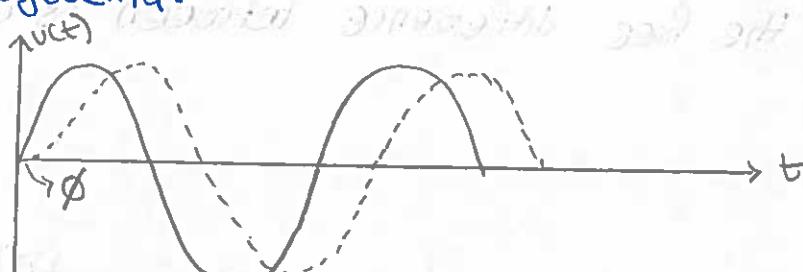
⇒ So, using this PLL, it is possible to generate the output frequency which is multiple of the input frequency.

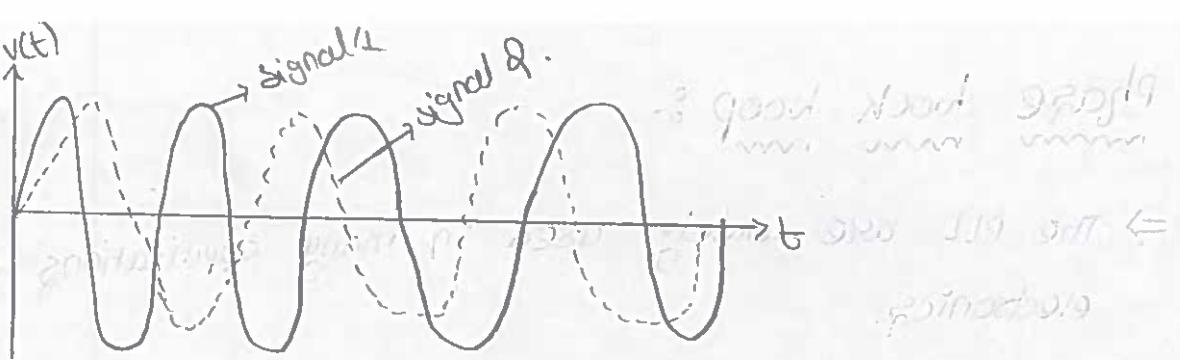
## Working of Phlo :-



⇒ As per name, it is the control system or the control loop which maintains the same phase b/w the ip and op signal.

⇒ In some systems we get some phase differences between the two signals at this time positive phase difference can be corrected by these type of systems.





⇒ In above figure, the two waveforms started at the same time, but there is a different frequency of the signals, here the phase between positive two signals continuously changing with time.

### Block diagram of PLL

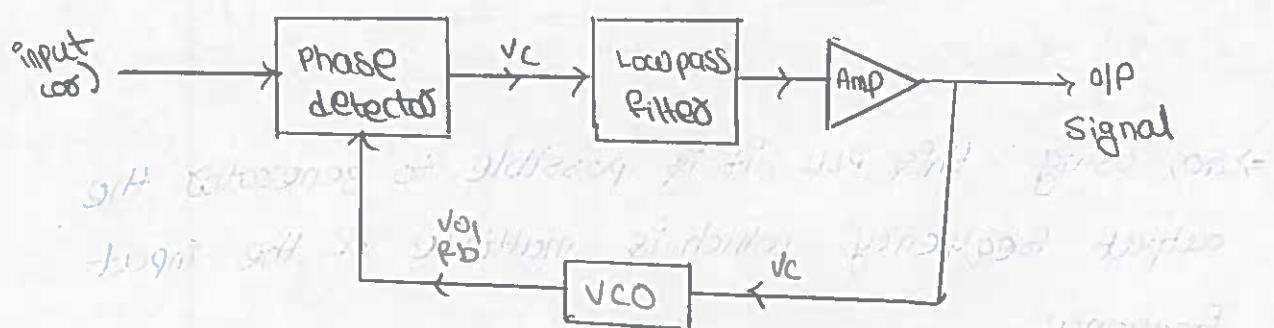


fig:- Block Diagram of PLL

- ⇒ The PLL consists of three basic building blocks. They are phase detector, low pass filter and vco-voltage controlled oscillator.
- ⇒ The vco as the control voltage changes, then the frequency of the oscillation also changes.
- ⇒ The phase detector is fundamentally a multiplier, and produces the sum ( $f_s + f_o$ ) and the difference ( $f_s - f_o$ ) components at its output.
- ⇒ The signal  $V_c$  shifts the vco free in a direction to reduce the free difference between  $f_s$  and  $f_o$ .

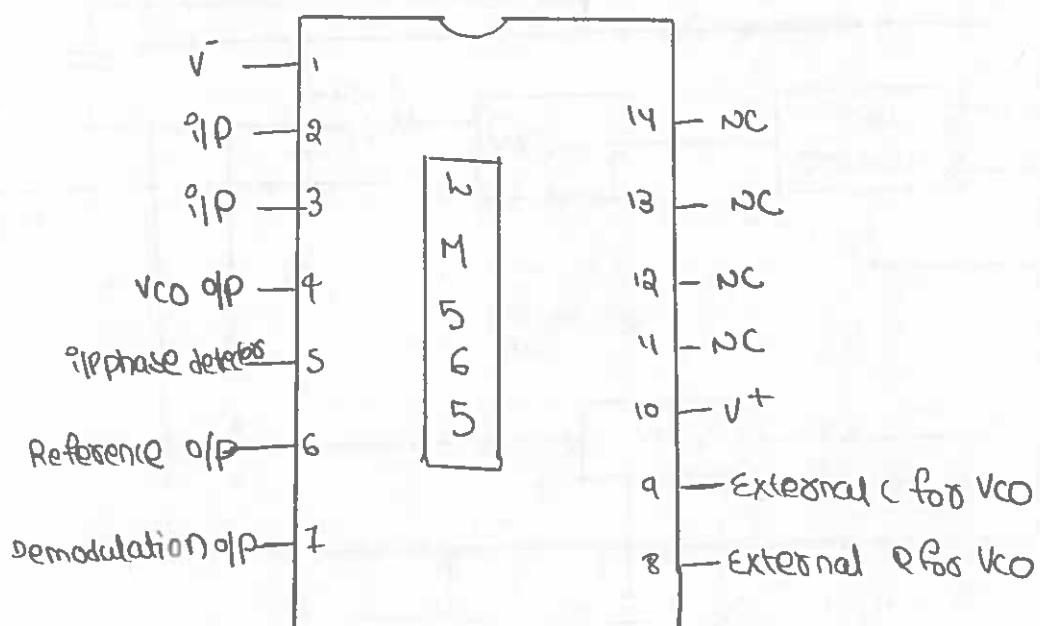


Fig 8 - Pin diagram of TC565

- \* The TC565 act as a PLL, and it is a 14 pin IC in dual in line package style.
- \* The PLL TC565 is usable over the frequency range 0-1Hz to 500KHz. It has highly stable control loop and is able to achieve a very linear FM detection.
- \* The o/p of VCO is capable of producing TTL compatible square wave.
- \* The dual supply is in the range of  $\pm 6V$  to  $\pm 12V$ .
- \* In this IC, dual power supply +V at pin 10 and -V at pin no 4.
- \* Pin 8 & 9 for the signal 9IP fed phase detector.
- \* Pin 4 & 5 are shorted externally so that VCO o/p is applied for phase detection. In some applications PLL loop is broken and some circuit is to connected b/w pin 4 & 5.
- \* Pin 6 Reference dc voltage is available.
- \* Pin 7 demodulated o/p. If 9IP signal b/w pin 8 & 3 is FM signal then at pin 7 we get FM demodulation output.
- \* Pin 8 & 9 external R<sub>1</sub> & C<sub>1</sub> for VCO.

Functional diagram of IC565 :-

IC565 - 2T WDT

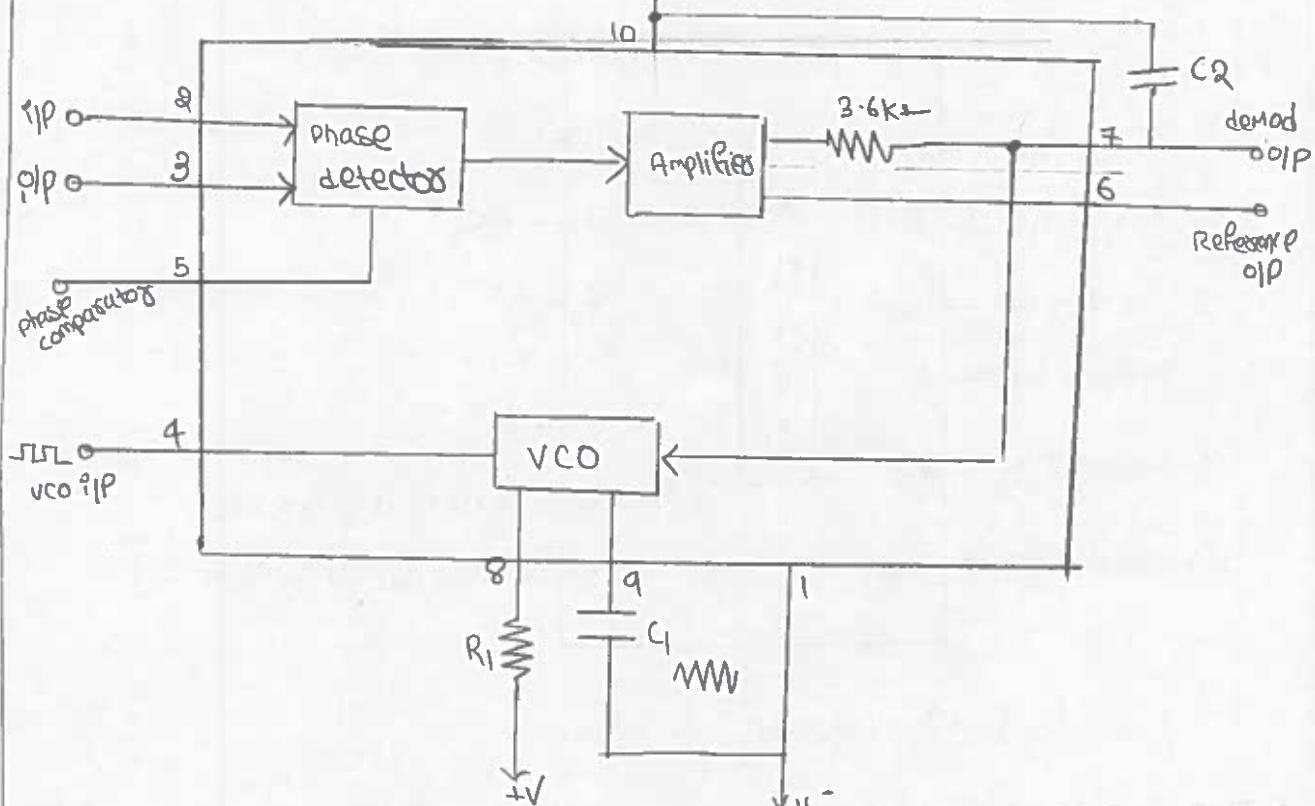


Fig 8 - Block diagram of IC565

- \* The free running frequency  $f_0$  at +ve VCO is determined by an externally connected resistor and timing capacitor ( $R, C_1$ ).
- \* When the loop is locked the free  $f_0$  is directly proportional to an externally applied voltage  $V_C$  called the DC control voltage.
- \* When an ilp periodic signal  $V_i$  of frequency  $f_i$  and VCO o/p signal  $V_o$  of frequency  $f_o$  are applied to the PLL, the phase detector produces a DC low frequency signal  $V_C$  which is proportional to the phase difference between the ilp signal  $V_i$  and the VCO o/p signal  $V_o$ .
- \* Once PLL locked, the PLL tracks the frequency changes of the input.
- \* This, PLL goes through 3 stages.
  - i, Free running range

ii, lock Range

iii, capture Range

Phase Detectors / comparators of Phs

These are two types of phase detectors.

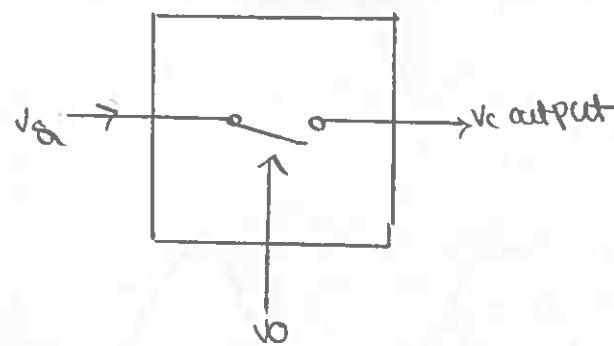
1. Analog phase detector

2. Digital phase detector

i, Analog phase detector

- The analog phase detector realized by using an electronic switch.
- Assuming that the signal from VCO generates the electronic switch, the PIP signal  $V_i^o$  is chopped by the VCO PIP.
- The V<sub>c</sub> and the filtered error  $V_{c,o}$  is the OIP square wave produce different values of filtered error voltages with respect to various values of phase errors  $\phi$ .  $V_c$  is shown as cross-hatched area in the given below waveform.

Electronic switch.



- the OIP of the phase detector when passed through the filter gives out an average error signal shown as denoted directly in the below waveform.
- The error voltage  $V_{c,o}$  is zero when the phase difference between the PIP's equal to  $90^\circ$ .
- The error voltage is  $V_c$  when the phase difference  $\phi$  is equal to  $0^\circ$  between the two input's.

when  $\phi_i = \phi_o$  at locked

$$V_C = \frac{KV^0 V_0}{\alpha} [\cos(\omega_i t - \omega_o t - \phi) - \cos(\omega_o t)]$$

$$V_C = \frac{KV^0 V_0}{\alpha} [\cos(-\phi) - \cos(\omega_i t + \phi)]$$

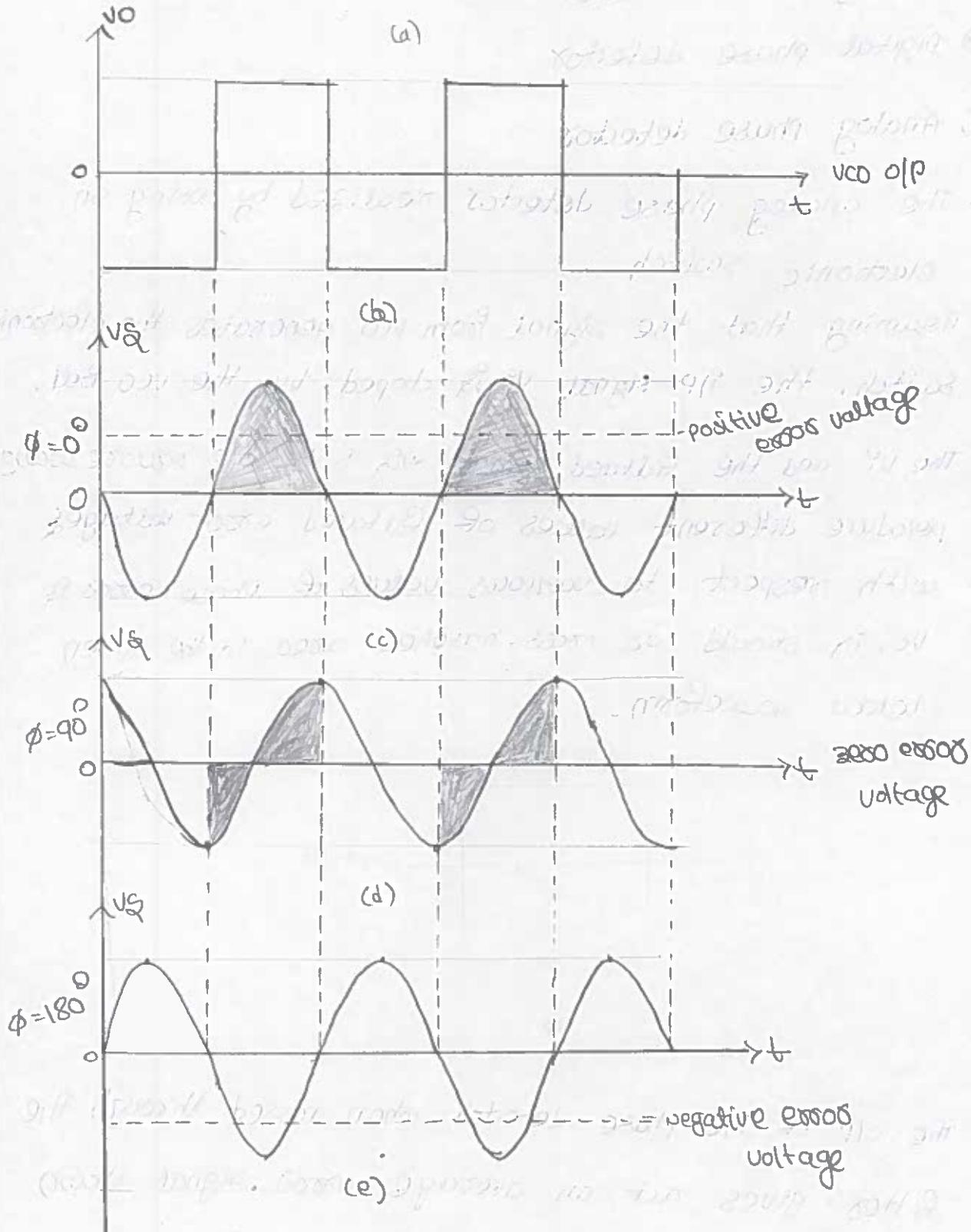


Fig:- Basic phase detector circuit & waveforms.

## Balanced Modulator Type Phase Detector :-

- \* The error voltage  $V_e$  is proportional to the input signal amplitude  $V_s$ . This is undesirable since it makes phase detector gain and the loop gain dependent on the input signal amplitude.
- \* The output is proportional to  $\cos \phi$  instead of only  $\phi$ . This makes it non-linear.
- ⇒ This problems can be eliminated by balanced modulator (or) Gilbert multiplication cell out.

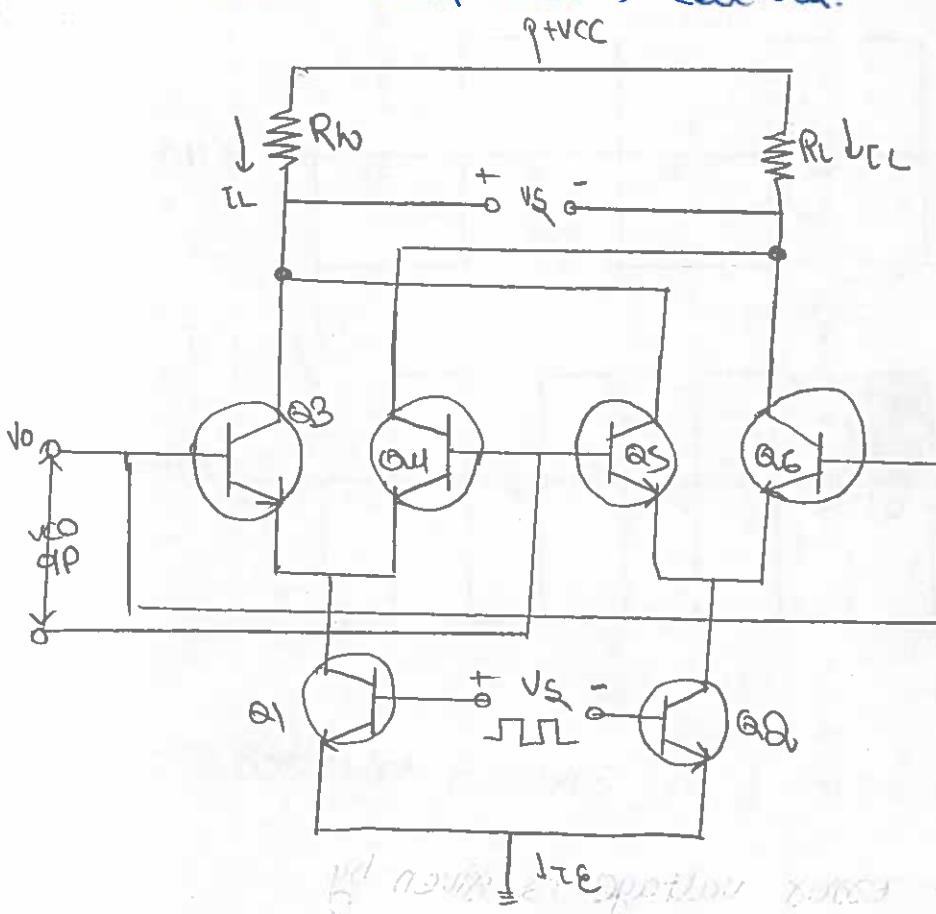


Fig :- Balanced Modulator Type Phase detector

- ⇒ The circuit diagram for the balanced modulator used as a full-wave switching phase detector.
- ⇒ The input signal  $V_s$  applied to the differential pair  $Q_1 - Q_2$ .
- ⇒ The transistor pairs  $Q_3 - Q_4$  and  $Q_5 - Q_6$  act as a single pole double throw switches.
- ⇒ These switches are controlled by the output signal from VCO.

$\Rightarrow$  The amplitudes of VCO signal and input signal are kept such that transistors are driven into saturation and cutoff so that they can act as closed switch and open switch, respectively.

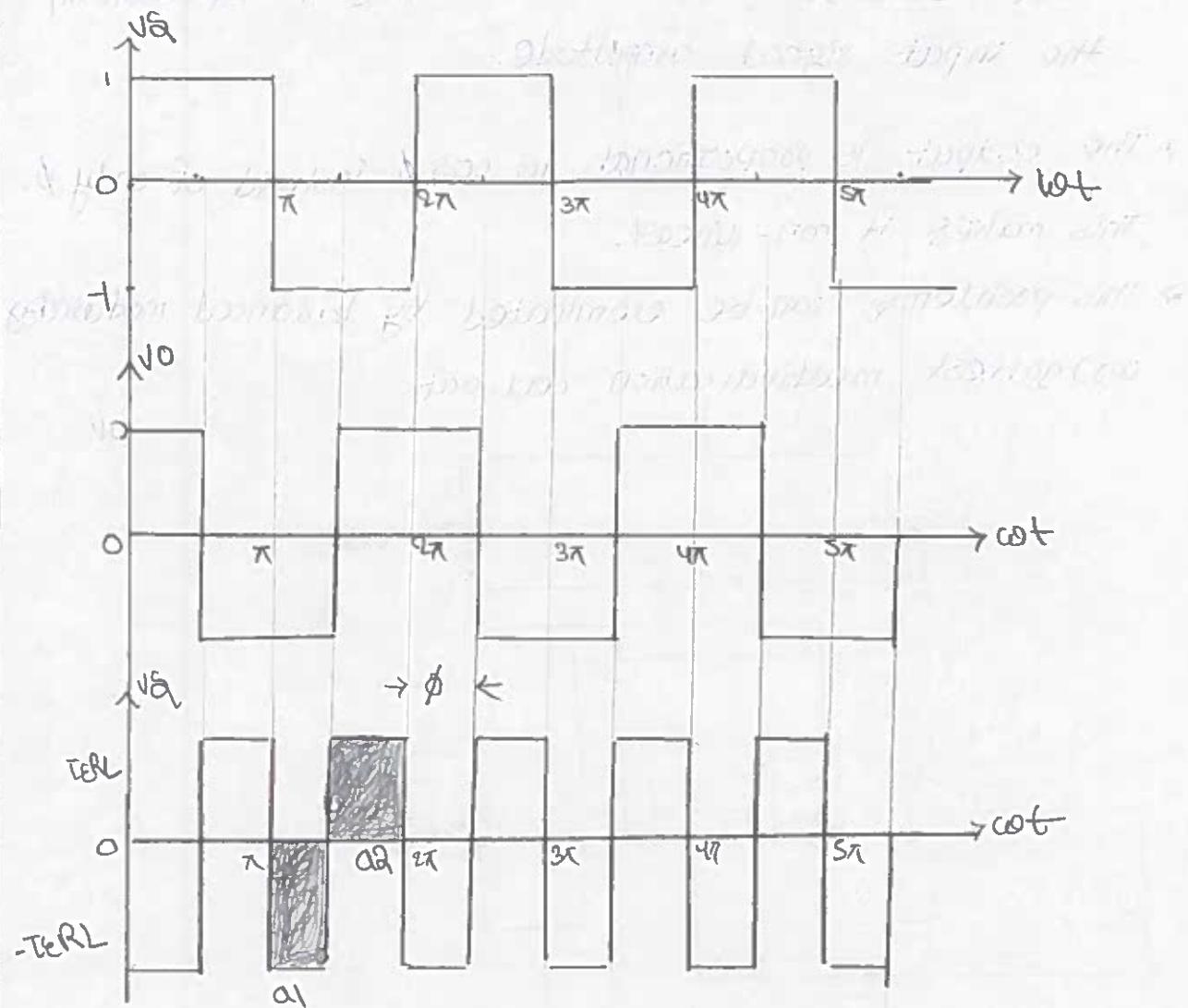


Fig :- waveforms of Balanced Modulator

The output error voltage  $V_E$  is given by

$$V_E = T_{RL}$$

\* It is positive when either  $Q_1$  and  $Q_4$  are ON or  $Q_2$  and  $Q_5$  are ON. It is negative when either  $Q_1$  and  $Q_3$  are ON or  $Q_2$  and  $Q_6$  are ON.

\* The average value of the output voltage of the phase detector,  $V_E$  can be obtained as

$$V_{EAV} = \frac{1}{\pi} (\alpha_1 + \alpha_2)$$

whole  $a_1$  : shaded area shown in the negative half  
 $a_2$  : shaded area shown in the positive half.

$$V_{\text{cov}} = \frac{1}{\pi} [(-\tau_{\text{ERL}})(\pi - \phi) + (\tau_{\text{ERL}})(\phi)]$$

$$= \frac{\tau_{\text{ERL}}}{\pi} (-\pi + \phi + \phi)$$

$$= \frac{2\tau_{\text{ERL}}}{\pi} \left[ \phi - \frac{\pi}{2} \right]$$

$$= \frac{4\tau_{\text{IRL}}}{\pi} \left[ \phi - \frac{\pi}{2} \right] \quad \because \tau_{\text{E}} = 2\tau_{\text{I}}$$

$$V_{\text{cov}} = k\phi \left[ \phi - \frac{\pi}{2} \right] \quad \because k\phi = \frac{4\tau_{\text{IRL}}}{\pi}$$

Digital Phase detector

\* Phase detector using XOR gate

\* Phase detector using RS flipflop.

i, Phase detector using X-OR gate

The XOR gate can be used as a digital phase detector when both signal  $f_s$  and  $f_o$  are square waves. This is illustrated in the diagram. We know that the output of XOR gate is high when only one of the input signals is high.

⇒ The input and output waveform for digital phase detector. Here  $f_s$  is leading  $f_o$  by  $\phi$  degrees.

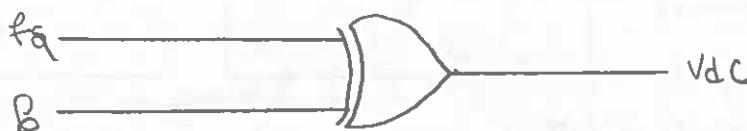


fig :- XOR gate as a digital phase detector.

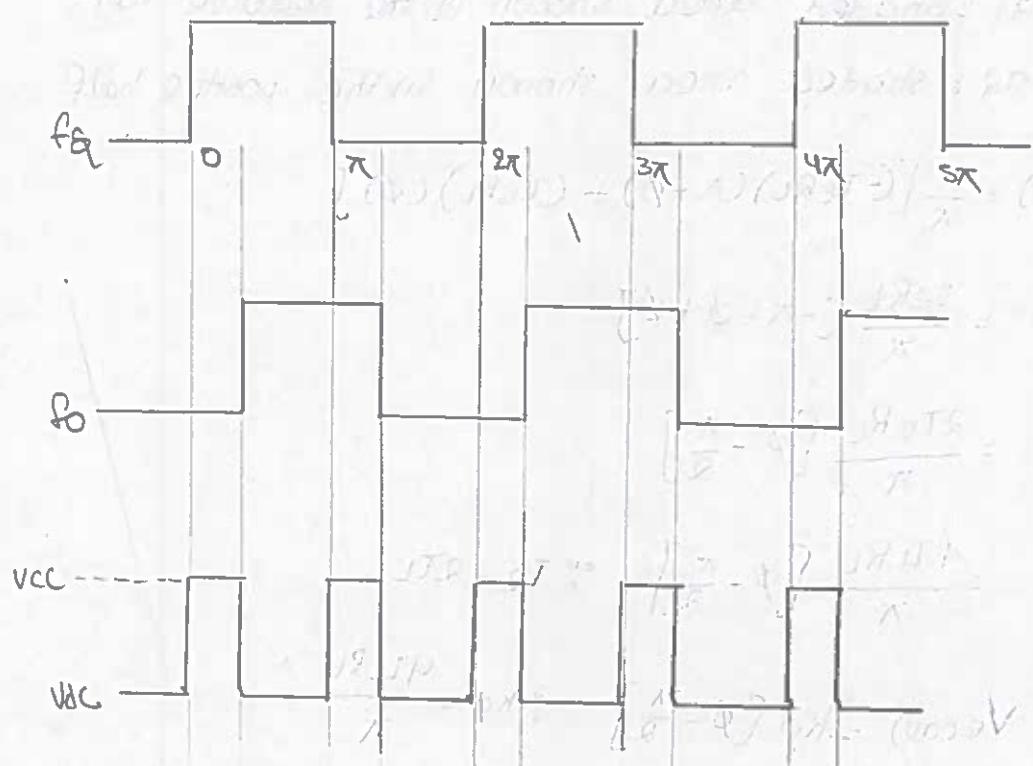


Fig :- IIP & OLP waveforms.

IIP, Phase Detector using RS Flip-Flop :-

- \* The digital phase detector using edge-triggered RS FF.
- \* The phase detector is used when  $f_s$  &  $f_o$  are both pulse waveforms with duty cycle less than 50%.
- \* The IIP  $f_q$  is connected to S input of the RS FF and the  $f_o$  is connected to R input of the RS Flip-Flop.
- \* At the rising edge of the input signal, OLP goes high and at the rising edge of the VCO OLP signal, output goes low.

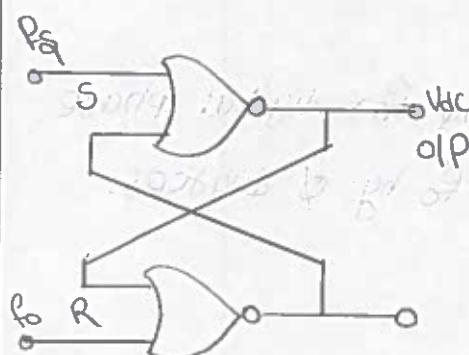


Fig :- Digital phase detector using RS flip-flop

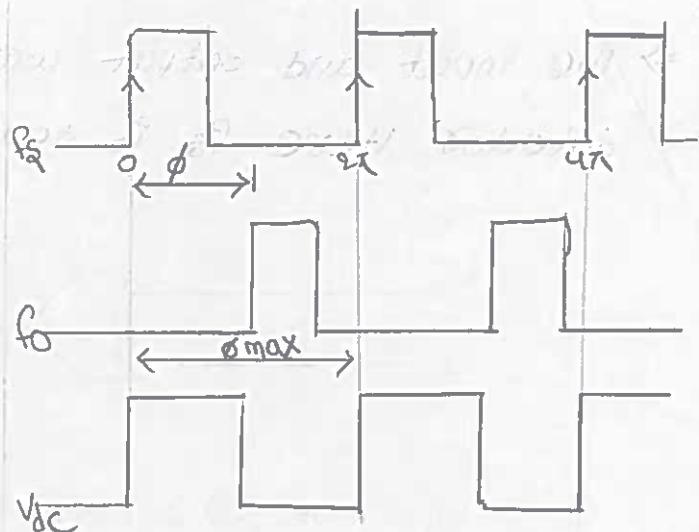


Fig :- IIP & OLP waveforms.